3. (Amended) The dynamic power management device [apparatus] of Claim 2, wherein said power control means comprises means for selecting between alternate power sources, [a switching regulator,] and means for feeding voltage information back to said logic control means.

4. (Amended) The dynamic power management device [apparatus] of Claim 3, wherein said voltage information includes both voltage output information used by said logic control means to cause said power control means to maintain a specified voltage output[,] and voltage source information used by said logic control means to cause said means for selecting to select one of said alternate power sources.

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5. (Amended) The dynamic power management device [apparatus] of Claim 2, wherein said logic control means comprises a DMA controller, a data sequencer, and a timing sequencer.

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6. (Amended) The dynamic power management device [apparatus] of Claim 10, wherein said logic control means further comprises refresh timer means for timing refresh intervals, a binary address generator, and an encoder, said logic control means [together for] generating said address signals for said memory integrated circuit.

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7. (Amended) The dynamic power management device [apparatus] of Claim 2, further comprising slew rate controller means for limiting the time rate of change of voltage of said control signals and said data signals transmitted [input] to said memory integrated circuit.

Sub 2
8. (Amended) The dynamic power management device [apparatus] of Claim 2, wherein said logic control means causes

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL
25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 283-1222
FAX (408) 283-1233

said power control means to supply to said memory integrated circuit a relatively low voltage during a standby period, a higher voltage during memory refresh, and a still higher voltage during memory access.

9. (Amended) The dynamic power management device [apparatus] of Claim 2, further comprising daisy chain controller means for enabling communication with another dynamic power management device.

10. (Amended) The dynamic power management device [apparatus] of Claim 2, wherein said logic control means is provided with a sleep mode for conserving power during periods of inactivity.

Please add the following new claims:

11. The dynamic power management device of Claim 2, wherein said I/O means further comprises error correction means for detecting and correcting errors in said parallel data signals.

12. The dynamic power management device of Claim 3, wherein said logic control means generates said control signals for data access activity when said power control means supplies a voltage high enough to perform the data access activity and does not generate said control signals for data access activity when said power supply means does not supply a voltage high enough to perform the data access activity.

13. The dynamic power management device of Claim 6, wherein said encoder is a Gray code encoder.

14. The dynamic power management device of Claim 4,

LAW OFFICES OF
BEJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL
25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 283-1222
FAX (408) 283-1233

wherein said power control means comprises a pulse width modulator circuit responsive to said logic control means for generating a pulse width modulated signal having pulses with pulse widths proportional to said specified voltage output.

15. The dynamic power management device of Claim 14, wherein said power control means further comprises a low pass filter, said low pass filter filtering said pulse width modulated signal.

16. The dynamic power management device of Claim 15, wherein said power control means further comprises a FET driver circuit, said FET driver circuit generating a variable voltage in response to said filtered pulse width modulated signal.

17. The dynamic power management device of Claim 1, wherein said power control means further comprises an internal voltage generator, said internal voltage generator generating a calibration voltage.

18. The dynamic power management device of Claim 4, wherein said logic control means controls said power control means to maintain said specified voltage output through closed loop monitoring of said voltage output information.

19. The dynamic power management device of Claim 1, wherein said dynamic power management device supplies power to a plurality of memory integrated circuits in said computer system.

20. The dynamic power management device of Claim 19, wherein said dynamic power management device further comprises a plurality of ports, each port of said plurality of ports coupled to one memory integrated circuit of said plurality of

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 283-1222
FAX (408) 283-1233

memory integrated circuits.

21. An integrated circuit for controlling the power supplied to a solid state memory integrated circuit having a first operation period, a second operation period, and a third operation period, said integrated circuit comprising:

power control means for supplying a variable voltage to said memory integrated circuit;

logic control means for causing said power control means to supply to said memory integrated circuit a first voltage during said first operation period, a second voltage different from said first voltage during said second operation period, and a third voltage different from said first and second voltage during said third operation period.

22. The integrated circuit of Claim 19, wherein said logic control means causes said memory integrated circuit to enter said first, second or third operation period only when said power control means supplies a voltage meeting the voltage requirements of said memory integrated circuit to enter said first, second or third operation period, respectively.

23. A dynamic power management device for supplying power to a solid state memory integrated circuit in a computer system having a power source providing a substantially constant voltage, said dynamic power management device comprising:

power control means coupled to said power source for supplying a variable voltage to said memory circuit, said variable voltage being less than or equal to said substantially constant voltage provided by said power source; and

logic control means for generating address and control signals for said memory integrated circuit and for

LAW OFFICES OF
BEJEREVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 283-1222
FAX (408) 283-1233